We claim

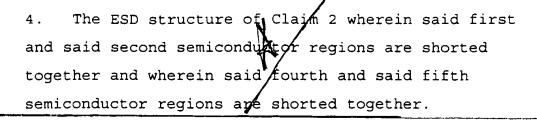
- 1. An electrostatic discharge (ESD) protection structure for protecting an Integrated Circuit comprising:
- a first semiconductor region of a first conductivity type;
  - a second semiconductor region of a second conductivity type adjacent said first semiconductor region;
- a third semiconductor region of a first conductivity type adjacent said second semiconductor region;
  - a fourth semiconductor region of a second conductivity type adjacent said third semiconductor region; and
  - a fifth semiconductor region of a first conductivity type adjacent said second fourth semiconductor region; wherein a first terminal, A, of said ESD structure is connected to said first semiconductor region and a second terminal, K, of said ESD structure is connected to said fifth semiconductor region.
  - 2. The ESD structure of Claim 1, wherein said first conductivity type is an n-type semiconductor and said second conductivity type is a p-type semiconductor.
  - 3. The ESD structure of Claim 1, wherein said first conductivity type is a p-type semiconductor and said second conductivity type is an n-type semiconductor.

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5. The ESD structure of Claim 4 wherein said third semiconductor region includes an n-well region formed in a p-type semiconductor substrate.

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6. The ESD structure of Claim 5 wherein said second and said fourth semiconductor regions each include a p-base region formed in said n-well region.

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- 7. The ESD structure of Claim 6 wherein said first and said fifth semiconductor regions each include an n<sup>+</sup> region formed in one of said p-base regions.
- 8. The ESD structure of Claim 1 further comprising a first current source connected across terminal A and a first end of a first resistor whose second end is connected to terminal K and a second current source connected across terminal K and a first end of a second resistor whose second end is connected to terminal A.

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9. The ESD structure of Claim 7 further comprising a first current source connected across terminal A and a first end of a first resistor whose second end is connected to terminal K and a second current source

connected across terminal K and a first end of a second resistor whose second end is connected to terminal A.

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10. The ESD structure of Claim 9 wherein said first and said second current sources each include a pair of back-to-back Zener diodes.

11. A method of protecting an Integrated Circuit against an electro-static discharge (ESD), said method comprising the steps of:

forming a first semiconductor region of a first conductivity type;

forming a second semiconductor region of a second conductivity type adjacent said first semiconductor region;

forming a third semiconductor region of a first conductivity type adjacent said second semiconductor region;

forming a fourth semiconductor region of a second conductivity type adjacent said third semiconductor region;

forming a fifth semiconductor region of a first conductivity type adjacent said fourth semiconductor region;

forming a first terminal over said first semiconductor region and in electrical contact therewith;

forming a second terminal over said fifth semiconductor region and in electrical contact therewith;

forming a low impedance conductive path across said two terminals.

- 12. The method of Claim 11 wherein the step of forming
  5 a third semiconductor region of a first conductivity
  type includes the step of forming an n-well region in a
  p-type substrate.
- 13. The method of Claim 12 wherein the steps of
  10 forming a second and a fourth semiconductor regions
  includes the steps of forming two separate and isolated
  p-type regions in said well.
- 14. The method of Claim 13 wherein the steps of forming a first and a fifth semiconductor regions includes the steps of forming a n-type semiconductor region in each of said p-type regions.
- 15. The method of Claim 14 further comprising means
  20 for varying a trigger voltage at which said forming a
  low impedance conductive path across said two terminals
  occurs.
- 16. The method of Claim 15 wherein said means includes
  25 a current source connected across said first terminal
  and a first end of a first resistor whose second end is
  connected to said second terminal and a second current
  source connected across said second terminal and a
  first end of a second resistor whose second end is
  30 connected to said first terminal.

17. The method of Claim 16 wherein said first and said second current sources each include a pair of back-to-back Zener diodes.

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18. An electrostatic discharge (ESD) protection structure comprising:

corner cells, each corner cell comprising a square-shaped semiconductor region of a first conductivity type surrounted on two sides by semiconductor regions of a second conductivity type, said first and said second semiconductor regions both formed in a second square-shaped semiconductor region of the first semiconductor conductivity type, said second square-shaped semiconductor region formed in a third square-shaped semiconductor region of a second conductivity type, said corner cells to form all corners of said ESD structure;

edge cells, each edge cell comprising a squareshaped semiconductor region of a first conductivity
type surrounded on three sides by semiconductor regions
of a second conductivity type, said first and said
second semiconductor regions both formed in a second
square-shaped semiconductor region of the first
semiconductor conductivity type, said second squareshaped semiconductor region formed in a third squareshaped semiconductor region of a second semiconductor
conductivity type, said corner cells to form all edges
of said ESD structure;

center cells, each center cell comprising a square-shaped semiconductor region of a first conductivity type surrounded on four sides by semiconductor regions of a second conductivity type, said first and said second semiconductor regions both formed in a second square-shaped semiconductor region of the first conductivity type, said second square-shaped semiconductor region formed in a third square-shaped semiconductor region formed in a third square-shaped semiconductor region of a second conductivity type, said center cells to form all portions of said ESD structure which are not formed by said corner cells and said edge cells.

- 19. The ESD protection structure of Claim 18 wherein said corner cells, said edge cells and said center cells have square geometrical shapes with identical areas.
- 20. The ESD protection structure of Claim 19 wherein said ESD protection structure has a square geometry.

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